Notice of Allowability	Application No.	Applicant(s)	
	10/015,180	JAIN ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/12/05*.

2. ☒ The allowed claim(s) is/are *1-44*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 12/16/05.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-44 were examined and allowed.

Section I: Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance:

While Dean (US Patent 5,553,276) teaches a method for enhancing dynamic timing simulation comprising: assessing a netlist comprising combinational logic nodes, including output nodes, interconnections, and input and output storage elements (claim 1);a computer readable medium containing executable instructions which, when executed in a processing system, causes the system to perform the steps for enhancing the runtime speed of a logical simulator, comprising: defining a combinational portion of a logic circuit as a network comprising nodes, including output nodes, interconnections, and input and output storage elements; assigning a delay to each of said nodes (claim 12); system comprising a processor coupled to a bus and memory coupled to said bus wherein said memory contains instructions that when executed on said processor implements a method of performing dynamic simulation, said method comprising: a performing a delay assessment on a netlist comprising gates and sequential cells, said delay assessment assigning delay information for respective nodes in said netlist (claim 39); a system for enhancing the runtime speed of a logic simulator comprising a computer system, said computer system further comprising instructions for: defining a combinational portion of a logic circuit as a network comprising nodes, including output nodes, interconnections, and input and output storage elements (claim 23); Khouja et al

(US 5,696,694) teaches a method of performing dynamic simulation comprising: performing a delay assessment on a netlist comprising and sequential cells, said delay assessment assigning information for respective nodes in said netlist; assigning zero delay to certain gates based on said delay information; and performing dynamic simulation with respect to gates having assigned thereto zero delay as indicated by (claim 33). None of these references, taken either alone or in combination, with the prior art of record disclose a determining a maximum forward delay sum for each node, including:

(claim 1) "determining a safe delay period for each of said output nodes; removing timing checks from those output nodes for which the maximum forward delay sum is less than the safe delay period; determining a minimum reverse delay difference for each of a portion of said nodes; identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward delay sum; setting the delays for the identified nodes to zero; and performing dynamic timing simulation"

(claim 12) "determining a maximum forward delay sum for each node; determining a safe delay period for each of said output nodes; removing timing checks from those output nodes for which the maximum forward delay sum is less than the safe delay period; determining a minimum reverse delay difference for each of a portion of said nodes; identifying the nodes for which the minimum reverse delay

difference is greater than the maximum forward delay sum; setting the delays for the identified nodes to zero; and compiling the logic simulator "

(claim 23) "assigning a delay to each of said nodes; determining a maximum forward delay sum for each node; determining a safe delay period for each of said output nodes; removing timing checks from those output nodes for which the maximum forward delay sum is less than the safe delay period; determining a minimum reverse delay difference for each of said interior nodes and said input nodes; identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward delay sum; setting the delays for the identified nodes to zero; and compiling the logic simulator"

(claim 33) "removing timing checks on sequential elements indicated as exempt from timing checks based on said delay information; assigning zero delay to certain gates based on said delay information; skipping timing checks for exempt sequential elements as indicated"

(claim 39) "removing timing checks on sequential elements indicated as exempt from timing checks based on said delay information; assigning zero delay to certain gates based on said delay information; and performing dynamic simulation on said netlist, wherein said dynamic simulation enhances performance by: performing cycle based simulation with respect to gates having assigned thereto zero delay as indicated by

; and skipping timing checks for exempt sequential elements as indicated by assigning zero delay to certain gates based on said del ay information".

3. While Dean or Khouja teach simulation of logic gates neither none of these references, taken either alone or in combination with the prior art of record disclose determining a maximum forward or minimum reverse delay sum and difference, respectively, for each node including: removing timing checks from output nodes, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art of record.

Examiner's Amendment

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The specification has been amended as follows:

Pg. 1, line 18, after the word" design", a period -- . – was inserted.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Drawings

4. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because for example, the fonts and handwriting for figures 3 and 6, respectively, are difficult to read. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Section II: Response to Applicants' Arguments (2nd Office Action)

112 2nd and 103(a)

5. Applicants are thanked for addressing these issues. Rejections are withdrawn.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

December 16, 2005

TS

Paul L. Rodriguez 12/22/05
Primary Examiner
Art Unit 2125